I, the undersigned, who have prepared English translation which is attached herewith, hereby declare that the aforementioned translation is true and correct translation of officially certified copy of the Korean Patent Application No. 2002-44986 filed on July 30, 2002.

February 23, 2005

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Suk-Cheol Yang

[Abstract of the Disclosure]

[Abstract]

The present invention is directed to a semiconductor capacitor including an upper electrode of a capacitor formed using physical vapor deposition (PVD) as well as chemical vapor deposition (CVD) and a method of forming the same. When the upper electrode of the capacitor is formed, a first upper electrode is formed using CVD and then a second upper electrode is formed using PVD or a first upper electrode is formed using PVD and then a second electrode is formed using CVD. Since the upper electrode of the capacitor is formed through two steps using CVD and PVD, it may be thickly formed at a high speed and an electric property of the upper electrode is not degraded.

[Typical Figure]

FIG. 3

[Index]

capacitor, CVD, PVD, cell area, peripheral circuit area

[Specification]

[Title of the Invention]

SEMICONDUCTOR CAPACITOR AND METHOD OF FORMING THE SAME

[Brief Description of the Drawings]

FIG. 1 is a cross-sectional view of a conventional semiconductor device including a concave capacitor.

FIG. 2 is a cross-sectional view of a semiconductor device including a concave capacitor according to the present invention.

FIG. 3 through FIG. 7 are cross-sectional views for explaining a method of forming a concave capacitor according to the present invention.

FIG. 10 is a graph of a leakage current characteristic depending on whether a substrate bias is applied when an upper electrode is formed using PVD.

*Explanation of the signs that are the main part of the drawings

20, 120: first interlayer dielectric 28, 128: second interlayer dielectric

40, 140: third interlayer dielectric

26a, 26b, 26c, 26d, 126a, 126b, 126c, 126d: contact formed in first interlayer dielectric

46a, 146a: contact formed in third interlayer dielectric

46b, 46c, 146b, 146c: contact formed in third and second interlayer dielectric

30, 130: lower electrode 32, 132: dielectric layer

34, 134a, 134b: upper electrode 36, 136: capacitor

[Detailed Description of the Invention]

[Object of the Invention]

[Field of the Invention and Prior Art related to the Invention]

The present invention relates to a semiconductor capacitor and a method of forming the same. More specifically, the present invention is directed to a semiconductor capacitor including an upper electrode of a capacitor formed using physical vapor deposition (PVD) as well as chemical vapor deposition (CVD) and a method of forming the same.

As integration density of semiconductor memory devices increases, an area of a memory cell storing 1 bit is decreasing. Unfortunately, a capacitor area cannot decrease in proportion to decrease of memory cells. This is because a charge capacity higher than a constant degree is necessary to a unit cell for the purpose of a sensing signal margin and a durability to soft error caused by α-particles. Many efforts have been made for keeping a capacitance (C) of a memory capacitor higher a suitable value in a limited cell area. Like $C=\varepsilon As/d$ (ε : dielectric constant, As : surface area of electrode, d : thickness of dielectric substance), one of the efforts is to reduce a thickness (d) of a dielectric substance; another is to increase a surface area (As) of electrode, and the third is to use materials of high dielectric constant (ε).

The first manner has a limitation because leakage current increases with reduction in thickness of a dielectric substance. Therefore, the second and third manners have been used. In the second manner, a capacitor has a 3-dimensional structure such as simple stacked structure, a concave structure, a cylindrical structure, and a multi-fin structure to increase a surface of an

electrode. In the third manner, materials of high dielectric constant, e.g., (Ba, Sr)TiO_3(BST), (Pb, Zr)TiO_3(PZT), and Ta_2O_3 have been used.

Cylindrical (or concave) capacitors have been suggested to avoid a lower electrode etching difficulty caused by with increase in stack height of a lower electrode in the stacked capacitor.

FIG. 1 is a cross-sectional view of a conventional semiconductor device including a concave capacitor. A reference number '70' denotes a cell region, and a reference number '80' denotes a peripheral circuit region.

Referring to FIG. 1, in the cell region 70 and the peripheral circuit region 80, a MOS transistor is disposed on a substrate 2 where a device isolation region 4 is formed. The MOS transistor includes a gate electrode 11 and a source and drain region 18. The gate electrode 11 has a polysilicon layer 8, a silicide layer 10, and a gate insulation layer 6 interposed therebetween. A spacer 14 is formed on a sidewall of the gate electrode 12. The source and drain region 18 includes a lightly doped impurity region 12 and a heavily doped impurity region 16.

A first interlayer dielectric 20 is stacked on a substrate including the MOS transistor. Contacts 26a, 26b, and 26c are formed to be in contact with the source and drain region 18 through the first interlayer dielectric 20, and a contact 26d is formed to be connected with the gate electrode. Each of the contacts 26a, 26b, 26c, and 26d includes a barrier metal 22 and a tungsten layer 24.

A second interlayer dielectric 28 is stacked on a first interlayer dielectric 20 including the contacts 26a, 26b, 26c, and 26d. A concave hole 29 is formed at the cell region 70 to expose the contact 26a through the second interlayer dielectric 28. A capacitor 36 is disposed in the concave hole 29 to be connected to the contact 26a. The capacitor includes a lower electrode 30, a dielectric layer 26a, and an upper electrode 34.

In the cell region 70, a contact 46a is formed to be electrically

connected to the upper electrode 30 of the capacitor 30 through the third interlayer dielectric 40. The contact 46a is connected to an interconnection 52a. A bitline contact 46b is formed to be electrically connected to the contact 26b through the third and second interlayer dielectrics 40 and 28. The bitline contact 46b is connected to a bitline 52b. On the other hand, in the peripheral circuit region 80, contacts 46c and 46d are formed to be electrically connected to contact 26c and 26d through the third and second interlayer dielectrics 40 and 28. The contacts 46c and 46d are connected to interconnections 52c and 52d, respectively. Each of the bitlines and interconnections 52a, 52b, 52c, and 52d includes a barrier metal 48 and a conductive layer 50.

In a semiconductor device having the foregoing concave (cylindrical) capacitor of a CUB (capacitor under bitline) structure, a third interlayer dielectric is etched to form the contact 46a, 46b, 46c, and 46d, thereby forming an opening 41a exposing a surface of the upper electrode 30. At the same time, the third and second interlayer dielectrics are etched to form an opening 41b exposing the contacts 26a, 26b, and 26c.

Since the opening 41b exposing the contacts 26b, 26c, and 26d is deeper than the opening 41a exposing the upper electrode 30, the upper electrode 34 may be overetched.

Therefore, there is a need for a method of forming an upper electrode fast and thickly to enhance a yield.

Data stored in a DRAM cell is reserved as the amount of charges stored in a capacitor. Periodical refresh operation is performed to keep the data. Namely, since the amount of stored charges is not lost during a refresh period such that a DRAM operates smoothly, there is a need for a capacitor where leakage current does not occur.

[Technical Object of the Invention]

Therefore, it is an object of the invention to provide a capacitor having a superior electrical property while fast forming an upper electrode of a capacitor and a method of forming the capacitor.

It is another object of the invention to provide a semiconductor device adopting the capacitor and a method of forming the same.

[Construction of the Invention]

In order to achieve these objects, the present invention provides a capacitor including a lower electrode, a dielectric layer stacked on the lower electrode, and an upper electrode formed on the dielectric layer using CVD or ALD (atomic layer deposition) and an upper electrode formed on the dielectric layer using PVD.

In this embodiment, after forming a first upper electrode using CVD or ALD, a second upper electrode may be formed using PVD. Alternatively, after forming a first upper electrode using PVD, a second upper electrode may be formed using CVD or ALD.

Particularly, in the case where an upper electrode is formed first using PVD, an upper electrode is preferably formed by supplying a power only to a target without applying a bias power to a substrate when the PVD is applied. In this case, a leakage current characteristic is advantageously improved.

The present invention will now be described more fully hereinafter with reference to attached drawings, wherein the same numerals denote the same components.

FIG. 2 is a cross-sectional view of a semiconductor device including a concave capacitor according to the present invention.

Referring to FIG. 2, in a cell region 170, a MOS transistor is disposed on a substrate 102 where a device isolation region 104 is formed. A MOS transistor includes a gate electrode 111 and a source and drain region

118. The gate electrode 111 has a polysilicon layer 108 and a silicide layer 110 with a gate insulation layer 106 interposed therebetween. A spacer 114 is formed on a sidewall of the gate electrode 111. The source and drain region 118 includes a lightly doped impurity region 112 and a heavily doped impurity region 116. A first interlayer dielectric 120 is stacked on a substrate including the MOS transistor. A storage contact 126a is formed to connect the source region 118 through the first interlayer dielectric 120, and a contact 126b is formed to connect the drain region 118. Each of the contacts 126a and 126b includes a barrier metal 122 and a tungsten layer 124. A second interlayer dielectric 128 is stacked on a first interlayer dielectric 120 including the contacts 126a and 126b. A concave hole 129 is formed to expose the storage contact 126a through the second interlayer dielectric 128. In the concave hole 129, a capacitor 136 is disposed to be connected to the storage contact 126a. The capacitor includes a lower electrode 130, a dielectric layer 132, a first upper electrode 134a, and a second upper electrode 134b. The first upper electrode 134a may be formed using CVD, and the second upper electrode 134b may be formed using PVD. Alternatively, the first upper electrode 134a may be formed using PVD, and the second upper electrode 134b may be formed using CVD. A third interlayer dielectric 140 is stacked on a second interlayer dielectric 128 where the capacitor 136 is formed. A contact 146a is formed to be electrically connected to the upper electrode 130 of the capacitor through the third interlayer dielectric. The contact 146a is connected to an interconnection 152a. A bitline contact 146b is formed to be electrically connected to the contact 126b. The bitline contact 146b is connected to a bitline 152b. The interconnection 152a and the bitline 152a include a barrier metal 148 and a conductive layer 150.

On the other hand, in a peripheral circuit region 180, a MOS transistor is formed on a substrate. A first interlayer dielectric 120 is

stacked on a substrate including the MOS transistor. Contacts 126c and 126d are formed to be the source and drain region 118 or the gate electrode 111 of the MOS transistor through the first interlayer dielectric 120. A second interlayer dielectric 128 and a third interlayer dielectric 140 are sequentially stacked on a first interlayer dielectric 120 where the contacts 126c and 126d are formed. Contacts 146c and 146d are formed to be electrically connected to the contacts 126c and 126d through the third interlayer dielectric 140 and the second interlayer dielectric 128. The contacts 146c and 146d are connected to interconnections 152c and 152d, respectively.

In the above-described structure, an upper electrodes is durable to an overetch even though an opening 141a exposing the upper electrodes 134a and 134b of a capacitor and an opening 141b exposing the contacts 126b, 126c, and 126d are formed at the same time. This is because the upper electrodes 134a and 134b is thick enough to endure the overetch.

A method of forming a capacitor having the foregoing structure will now be described more fully with reference to FIG. 3 through FIG. 7.

Referring to FIG. 3, a device isolation layer 104 is formed to define an active region in a substrate 102. After sequentially stacking a gate insulation layer 104, a gate conductive layer 108, and a silicide layer 110 on a substrate where the device isolation region 104 is formed, they are patterned to form a gate electrode 111 with a gate insulation layer 104 interposed therebetween. Using the gate electrode 111 and the device isolation region 104 as an ion implanting mask, a lightly doped impurity region 112 is formed at the active region of the substrate. A space insulation layer is formed on an entire surface of a substrate where a gate electrode 111 is formed. The space insulation layer is anisotropically etched to form a spacer 114 on a sidewall of the gate electrode 111. Using the gate electrode 111 where the spacer 114 is formed and the device as an

ion implanting mask, a heavily doped impurity region 116 is formed on the active region of the substrate. The lightly and heavily doped impurity regions 112 and 116 becomes a source and drain region 118 of an MOS transistor. After stacking a first interlayer dielectric 120 on an entire surface of a substrate where a MOS transistor is formed, it is selectively etched to form an opening 125 exposing the source and drain region 118. A barrier metal 122 and a tungsten layer 124 are stacked in the opening 125 and on the first interlayer dielectric 120 and are chemically mechanically polished down to a top surface of the first interlayer dielectric to form contacts 126a and 126b filling the opening. After stacking a second interlayer dielectric 128 on a first interlayer dielectric 120 including the contacts 126a and 126b, the second interlayer dielectric 128 is etched using a typical photolithographic process to form an opening 129 exposing top surfaces of the contacts 126a and 126b.

A lower electrode conductive layer 130 is conformally formed in the opening 128 and on the second interlayer dielectric 128. The lower electrode conductive layer 130 may be made of one selected from the group consisting of metal nitride such as polysilicon, titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), and combinations thereof and noble metals such as ruthenium (Ru), platinum (Pt), iridium (Ir), and combinations thereof to a thickness of 50-2000 angstroms.

Referring to FIG. 4, a sacrificial layer 131 is formed on the lower electrode conductive layer 130 to sufficiently fill the opening 129. The sacrificial layer 131 is made of photoresist or oxide. The sacrificial layer 131 and the lower electrode conductive layer 130 are etched down to a top surface of the second interlayer dielectric 128 to form a lower electrode pattern. After formation of the lower electrode pattern 130, a wet cleaning process or an annealing process may be formed under an ambient containing oxygen or nitrogen such as NH_3, N_2 plasma or the like.

Referring to FIG. 5, a sacrificial layer 131 remaining in the opening is removed using a wet or dry etch. A dielectric layer 132 is conformally formed on the lower electrode pattern 130 and the second interlayer dielectric 128. The dielectric layer 132 may made of one selected from the group consisting of silicon oxide (SiO_2), silicon nitride (SiN), aluminum oxide (AlO), tantalum oxide (TaO), titanium oxide (TiO), hafnium oxide (HfO), zirconium oxide (ZrO), BST, PZT, and combinations thereof to a thickness of 10-1000 angstroms. After formation of the dielectric layer 132, an annealing process may be performed under an oxygen-containing gas ambient of O_2, O_3, N_2O, and H_2O or an inert gas ambient of N_2 or Ar.

Referring to FIG. 6, a first upper electrode 134a is conformally formed on the dielectric layer 132. The first upper electrode 134a may be made of one selected from the group consisting of metal nitride such as polysilicon, titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), and combinations thereof and noble metals such as ruthenium (Ru), platinum (Pt), iridium (Ir), and combinations thereof to a thickness of 100-2000 angstroms. The formation of the first upper electrode 134 is done using CVD or PVD.

Referring to FIG. 7, a second upper electrode 134b is formed on the first upper electrode 134a. A method of forming the second upper electrode 134b varies with a method of forming the first upper electrode 134a. That is, if the upper electrode 134a is formed using CVD or ALD, the second upper electrode is made of PVD. Unlike this, the upper electrode 134a is formed through two steps using CVD (or ALD) and PVD to an upper electrode thickly and conformally at a high speed. An anti-reflecting layer 137 made of silicon nitride or silicon oxide may be formed on the second upper electrode 134b. The anti-reflecting layer 137 may act as an etch-stop layer and may have a thickness of 400-500 angstroms.

Referring to FIG. 8, a third interlayer dielectric 140 is formed on a

second interlayer dielectric 128 where the capacitor 136 is formed. The third interlayer dielectric 140 is selectively etched to form an opening 141a exposing the upper electrode 134b of the capacitor. At the same time, the third interlayer dielectric 140 and the second interlayer dielectric 120 are etched to form an opening 141b exposing the contact 126b. The opening 141a exposing the upper electrode is overetched. But since the upper electrodes 134a and 134b are formed using PVD and CVD (or ALD) to have a sufficient thickness, it is durable to the overetch.

Referring to FIG. 9, a barrier metal 142 and a tungsten layer 144 are stacked in the openings 141a and 141b and on the third interlayer dielectric 140 and are chemically mechanically polished down to a top surface of the third interlayer dielectric to form contacts 146a and 146b. A barrier metal 148 and a conductive layer 150 are stacked on a third interlayer dielectric including the contacts 146a and 146b and are patterned to form an interconnection 152a and a bitline 152b.

As previously stated, the capacitor 136 includes a lower electrode 130, a dielectric layer 132, a first upper electrode 134a, and a second upper electrode 134b. The upper electrode is formed using CVD (or ALD) as well as PVD. That is, after forming a first upper electrode using CVD or ALD, a second upper electrode is formed using PVD. Alternatively, after forming a first upper electrode using PVD, a second upper electrode is formed using CVD or ALD.

In the case where a first upper electrode is formed using PVD and a second upper electrode is formed using CVD, a data retention characteristic based on time of data "0" is superior in test. On the other hand, when a negative voltage is applied, leakage current increases to deteriorate data retention characteristic based on time of data "1".

It is suggested that such a deterioration phenomenon, i.e., increase of leakage current, is caused by plasma damage occurring when a first upper

electrode is formed using PVD. Therefore, measurement of leakage current was done in the case where a bias power is applied only to a target except a substrate and in the case where a bias power is applied to a target as well as a substrate, when a first upper electrode is formed using PVD.

A capacitor used in the test was formed under the following conditions.

A lower electrode is formed in a concave hole whose height is 8000 angstroms, a width of a minor axis is 0.2 micrometer, and a width of a major axis is 0.6 micrometer. A method of forming the lower electrode is that titanium nitride (TiN) is formed using MOCVD to a thickness of 200 angstroms.

Tantalum oxide (TaO), acting as a dielectric layer, was deposited on the lower electrode to a thickness of 60 angstroms. After an annealing process was performed under ozone (O_3) ambient, tantalum nitride was deposited to a thickness of 90 angstroms and an annealing process was performed under ozone (O_3) ambient.

Titanium nitride, acting as a first upper electrode, was formed on the dielectric layer using PVD to a thickness of 800 angstroms. A process was performed in the case where a bias voltage is applied to a substrate and in the case where a bias voltage is not applied thereto, when a first upper electrode is formed using PVD.

Titanium nitride (TiN), acting as a second upper electrode, was formed on the first upper electrode using MOCVD to a thickness of 400 angstroms.

FIG. 10 is a graph of a leakage current characteristic measured under the foregoing condition.

The graph shows that the leakage current characteristic was more improved at a capacitor Plasma-2 than at a capacitor Plasma-1. The capacitor Plasma-2 is a capacitor where a first upper electrode is formed

without applying a bias power to a substrate, and the capacitor Plasma-1 is a capacitor where a first upper electrode is formed by applying a bias power to a substrate.

A table [Table 1] shows comparatively deposition thicknesses of a first upper electrode (hereinafter referred to as "PVD-TiN") and a second upper electrode (hereinafter referred to as "CVD-TiN") at a sidewall of a minor axis of a concave hole and a bottom of the concave hole under the foregoing condition.

[Table 1]

thickness of upper electrode (Å)		when a substrate bias is applied to PVD-TiN (Plasma-1)		when a substrate bias is not applied to PVD-TiN (Plasma-2)	
thickness of sidewall adjacent to bottom of concave hole (Å)	PVD-TiN	400	~0	470	70
	CVD-TiN		400		400
thickness of bottom (Å)	PVD-TiN	590	390	510	310
	CVD-TiN		200		200

As illustrated in the table [Table 1], when a first upper electrode PVD-TiN is formed, second upper electrodes CVD-TiN have the same thickness (400 and 200 angstroms, respectively) at a sidewall and a bottom of a concave hole irrespective of whether a substrate bias is applied.

However, the upper electrodes PVD-TiN have different thicknesses. That is, PVD-TiN of 70 angstroms is formed on a sidewall of a concave hole at the first upper electrode Plasma-2 while PVD-TiN is rarely formed on a sidewall of a concave hole at the first upper electrode Plasma-1.

As a result, since the second upper electrode PVD-TiN is formed on

a sidewall of a concave hole in case of Plasma-2, a leakage current characteristic is improved. That is, PVD-TiN has a higher purity than CVD-TiN, and the PVD-TiN is fully deposited in the concave hole to improve the leakage current characteristic.

As illustrated in the table [Table 1], an upper electrode is formed more thinly on a bottom of the concave hole in case of Plasm-2 than in case of Plasma-1. As a concave hole becomes narrower and an upper electrode deposited on a bottom becomes thicker, lifting of the upper electrode may occur more frequently at the bottom of the concave hole. In case of the Plasm-2, a relatively thin upper electrode may be formed on the bottom of the concave hole to suppress occurrence of the lifting.

[Effect of the Invention]

According to the present invention, when a concave or cylindrical capacitor is formed, an upper electrode is formed using two steps of CVD and PVD. Thus, the upper electrode is thickly formed at a high speed without deterioration of electrical property.

[Scope of the Claim]

[Claim 1]

A capacitor comprising:

a lower electrode formed on a substrate;

a dielectric layer stacked on the lower electrode; and

an upper electrode formed on the dielectric layer using CVD and an upper electrode formed on the dielectric layer using PVD.

2. The capacitor of claim 1, wherein the CVD-formed upper electrode and the PVD-formed upper electrode are made of one selected from the group consisting of titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), ruthenium (Ru), platinum (Pt), iridium (Ir), and combinations thereof.

3. The capacitor of claim 1, wherein the upper electrode includes a CVD-formed upper electrode and a PVD-formed upper electrode which are stacked in the order named.

4. The capacitor of claim 1, wherein the upper electrode includes a PVD-formed upper electrode and a CVD-formed upper electrode which are stacked in the order named.

5. The capacitor of claim 1 being a concave capacitor.

6. A method of forming a capacitor, comprising steps of:

forming a lower electrode of a cylindrical capacitor on a substrate;

forming a dielectric layer on the lower electrode; and

forming an upper electrode on the dielectric layer using CVD as well as PVD.

7. The method of claim 6, wherein the upper electrode is made of one selected from the group consisting of titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), ruthenium (Ru), platinum (Pt), iridium (Ir), and combinations thereof.

8. The method of claim 6, wherein the step of forming the upper electrode comprises the steps of forming a first upper electrode using CVD and forming a second upper electrode using PVD.

9. The method of claim 6, wherein the step of forming the upper electrode comprises the steps of forming a first upper electrode using PVD and forming a second upper electrode using CVD.

10. The method of claim 9, wherein when the first upper electrode is formed using the PVD, a bias power is applied only to a target.

11. A method of forming a capacitor, comprising the steps of:

forming an interlayer dielectric on a substrate where a conductive region is formed;

selectively etching the interlayer dielectric to form a concave hole exposing the conductive region;

forming a lower electrode conductive layer in the concave hole and on the interlayer dielectric;

patterning the lower electrode conductive layer to form a lower electrode pattern on a bottom and a sidewall of the concave hole;

forming a dielectric layer on the lower electrode pattern;

forming a first upper electrode on the dielectric layer using PVD; and

forming a second upper electrode on the first upper electrode.

12. The method of claim 11, wherein the step of forming the first upper electrode using the PVD comprises a step of supplying a bias power only to a target.

13. The method of claim 11, wherein the second electrode is formed using CVD or ALD.

14. A method of forming a semiconductor device, comprising the steps of:

forming a first interlayer dielectric on a substrate where a MOS transistor is formed;

forming a first opening exposing a drain region of the MOS transistor through the first interlayer dielectric and a second opening exposing a source region of the MOS transistor;

filling the first and second openings with a conductive material to form a first contact and a second contact;

forming a concave hole exposing the first contact through the second interlayer dielectric;

conformally forming a lower electrode conductive layer in the concave hole and on the second interlayer dielectric;

forming a dielectric layer on the lower electrode; and

forming an upper electrode on the dielectric layer using PVD and CVD.

15. The method of claim 14, further comprising the steps of:

forming a third interlayer dielectric on a second interlayer dielectric where the capacitor is formed;

forming a third opening exposing the upper electrode of the capacitor through the third interlayer dielectric and a fourth opening exposing the second contact; and

filling the third and fourth openings with a conductive material to form a third contact and a fourth contact.

16. The method of 14, wherein the upper electrode is formed by forming a first upper electrode using CVD and forming a second upper electrode using PVD.

17. The method of 14, wherein the upper electrode is formed by forming a first upper electrode using PVD and forming a second upper electrode using CVD.

18. The method of claim 17, wherein when the first upper electrode is formed using the PVD, a bias power is applied only to a target.

Fig. 1

(PRIOR ART)

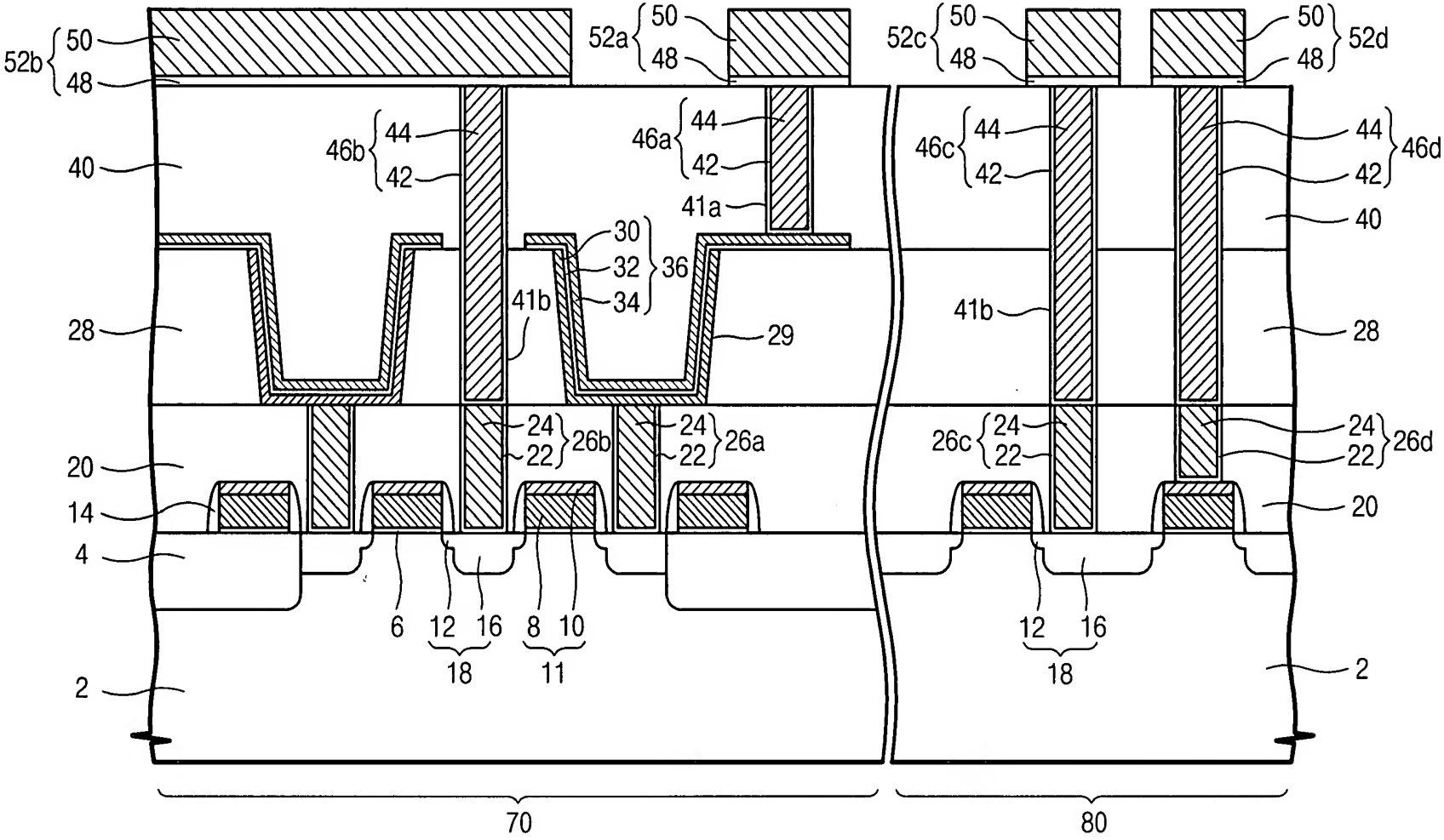

Fig. 2

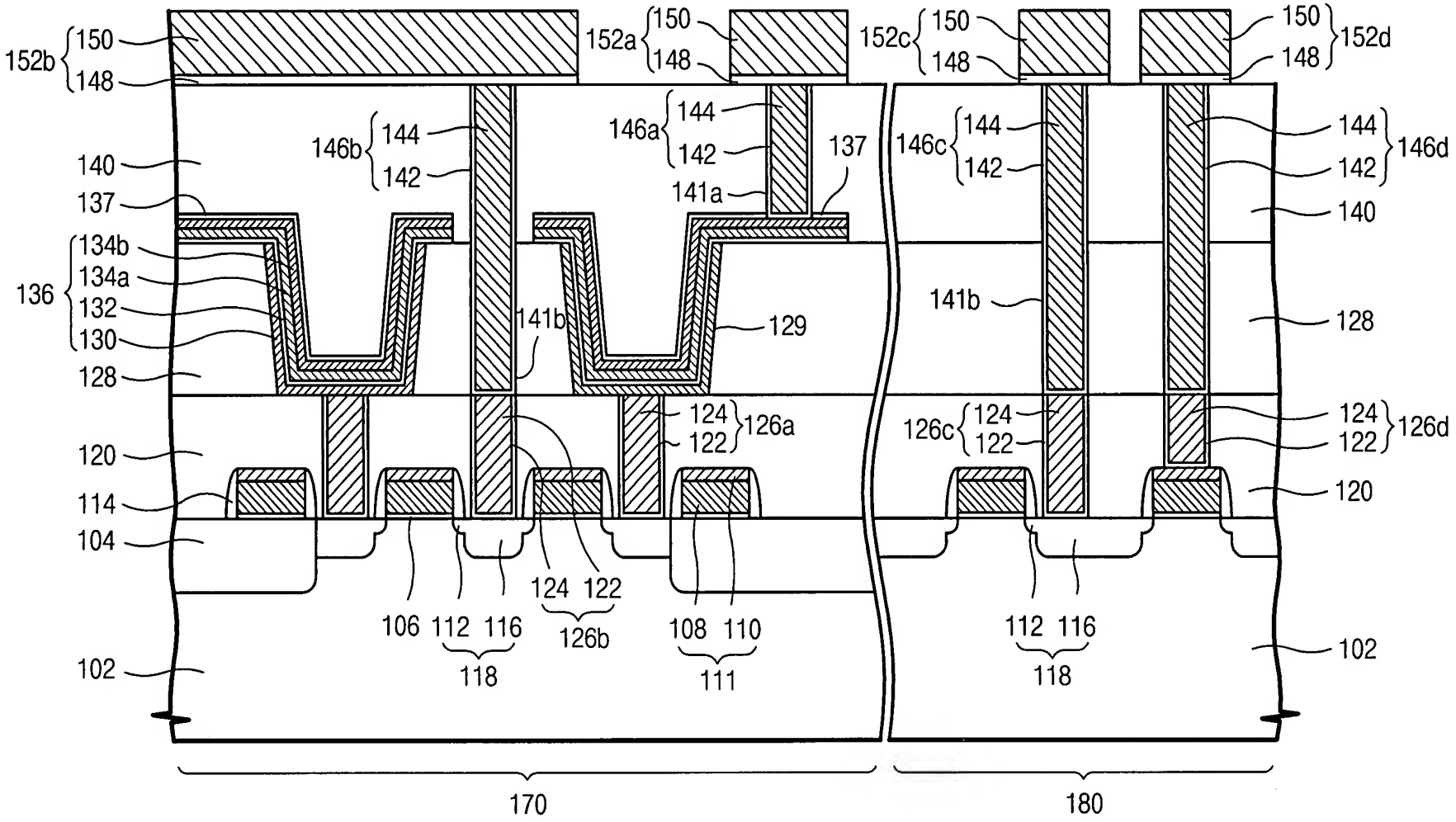
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Fig. 3

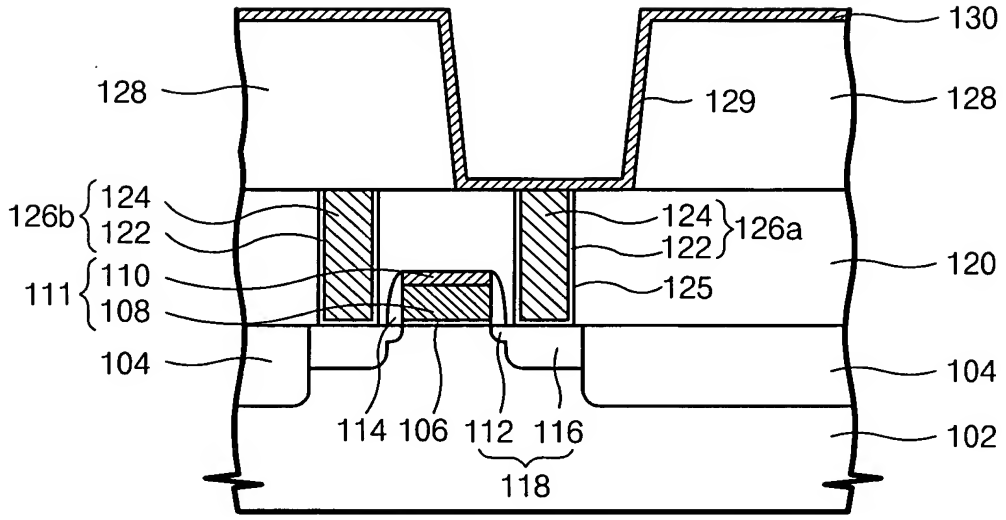
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Fig. 4

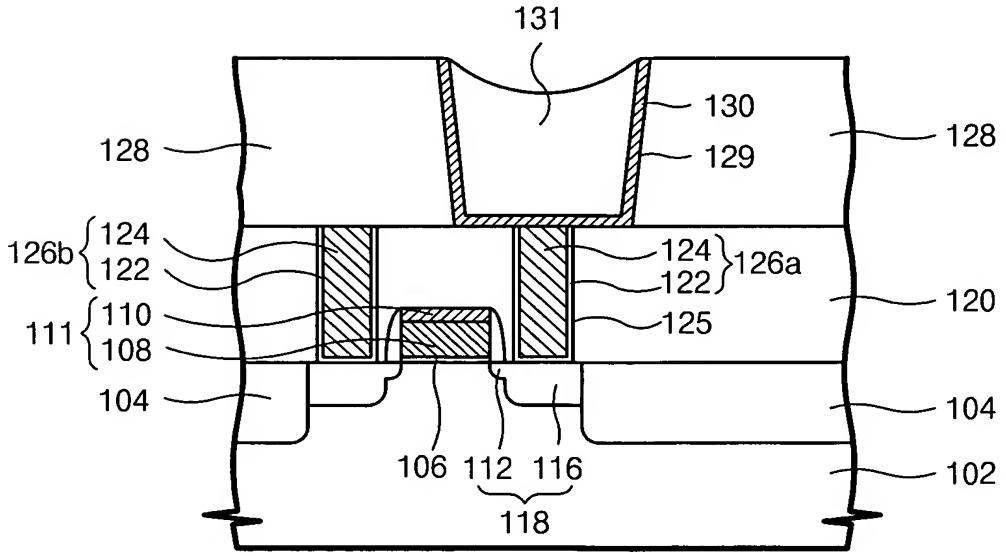
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Fig. 5

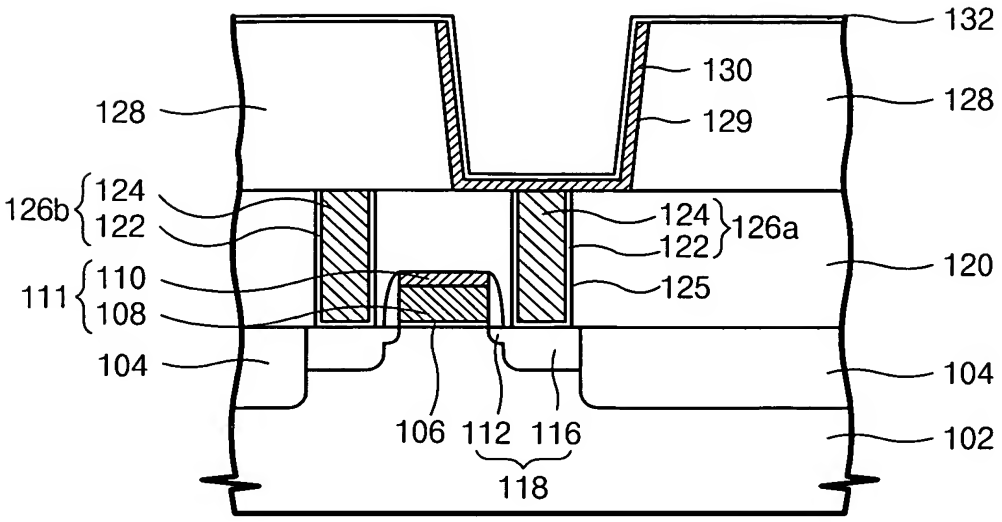
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Fig. 6

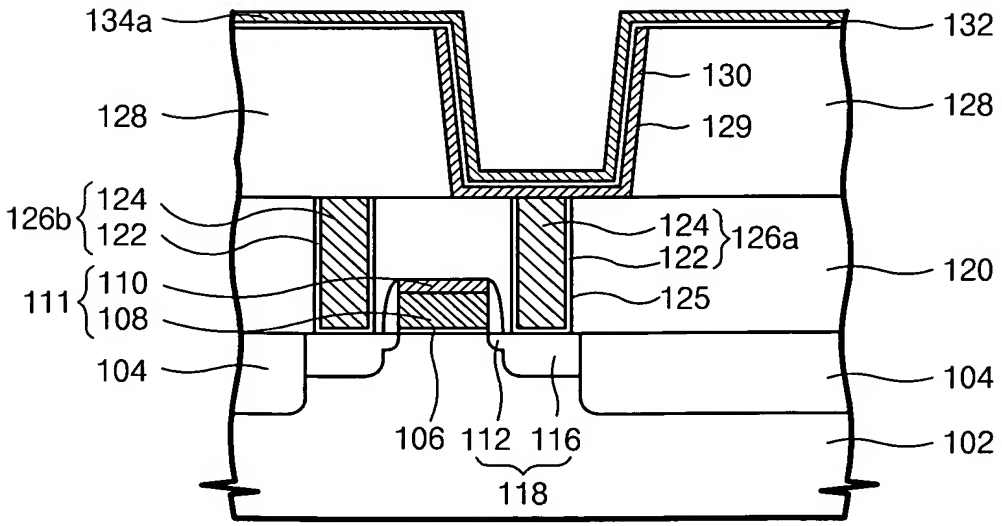
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Fig. 7

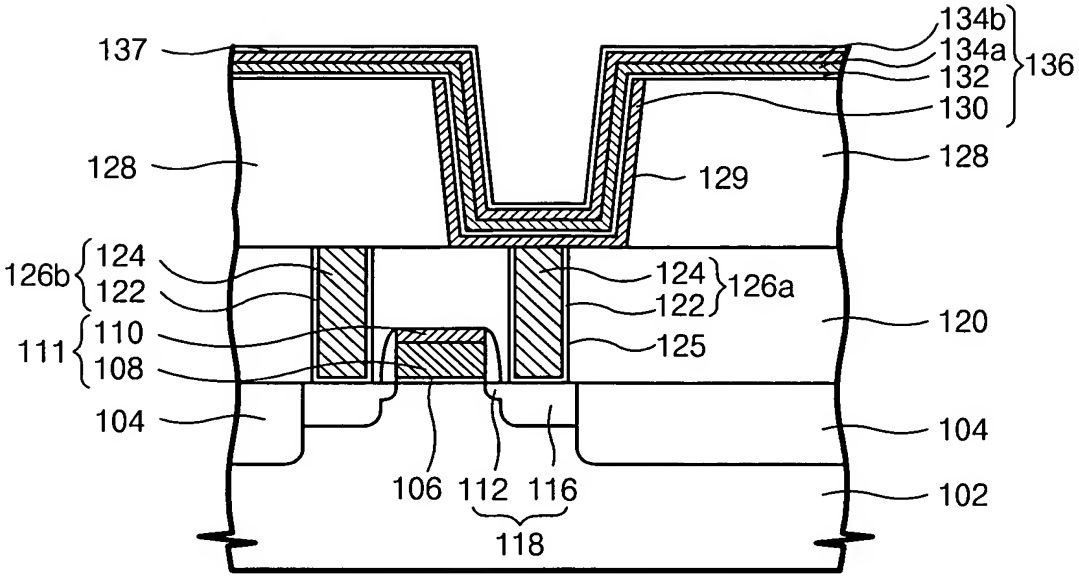
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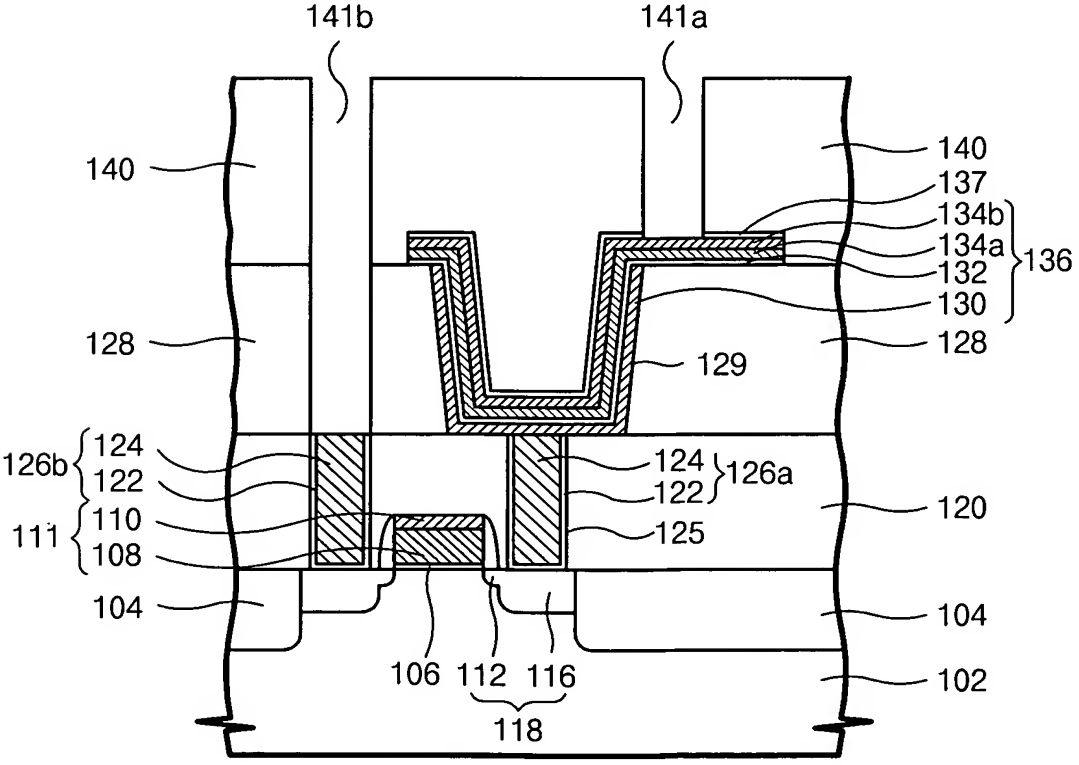
Fig. 8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102
118

Fig. 9

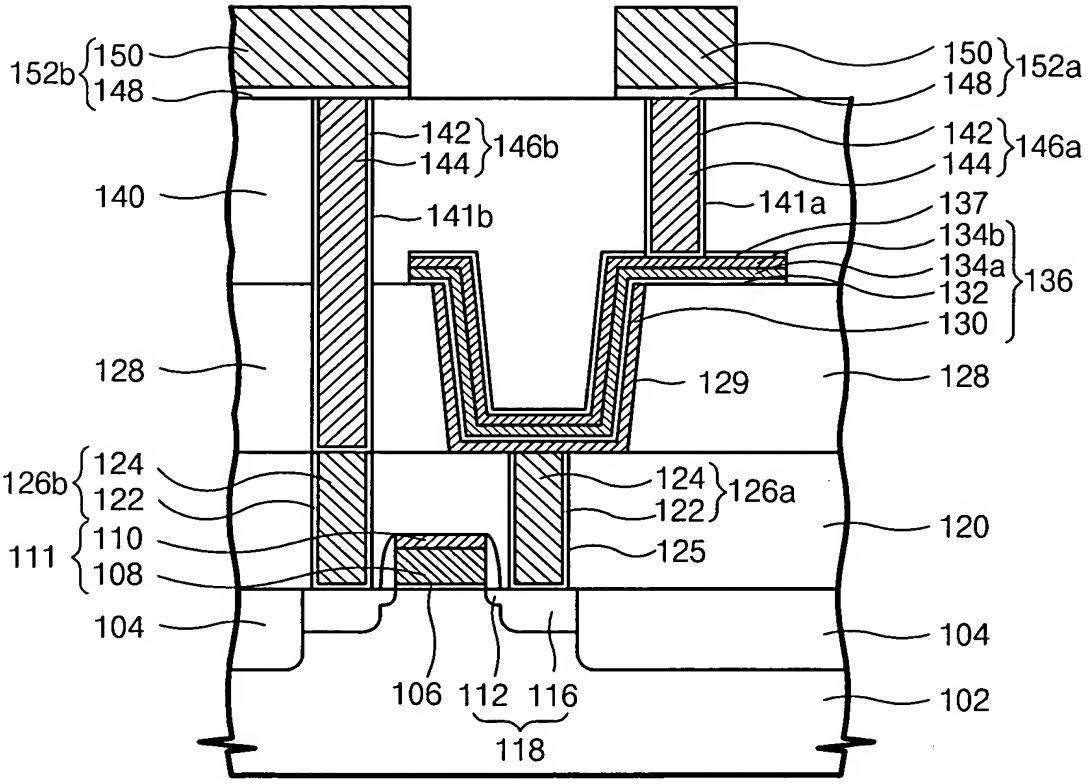
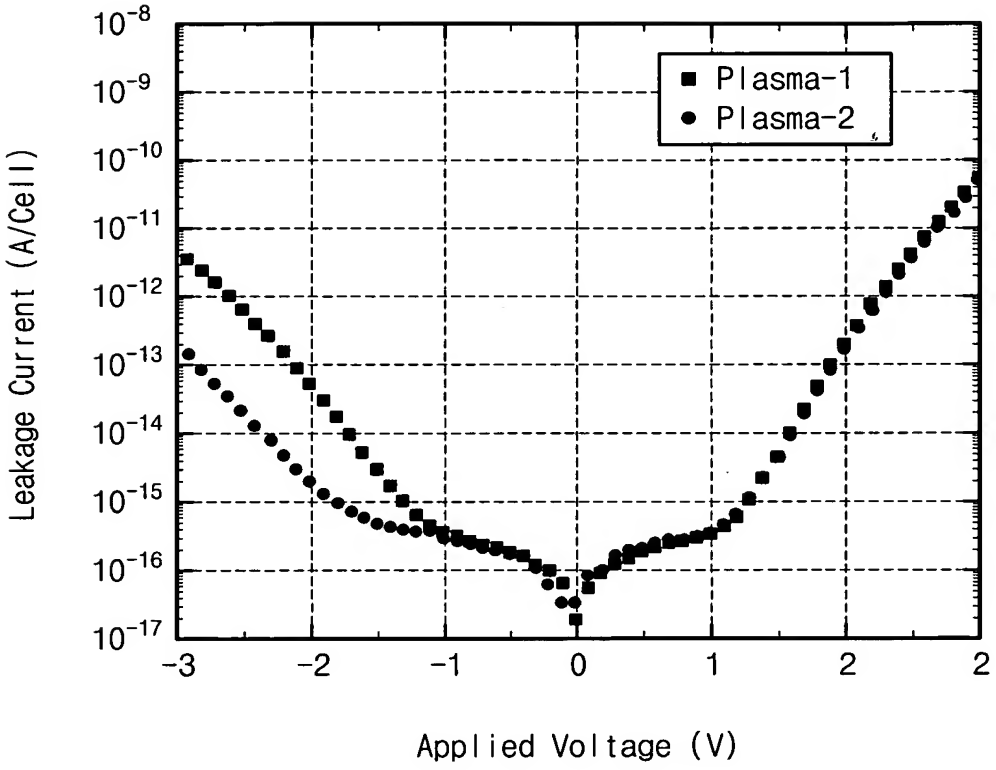

152b
150
148
142
144
146b
140
141b
128
126b
124
122
111
110
108
104
106
112
116
118
150
148
152a
142
144
146a
141a
137
134b
134a
132
136
130
129
128
124
122
126a
125
120
104
102

Fig. 10


Plasma-1
Plasma-2
Leakage Current (A/Cell)
Applied Voltage (V)
10^-8
10^-9
10^-10
10^-11
10^-12
10^-13
10^-14
10^-15
10^-16
10^-17
-3
-2
-1
0
1
2
2